

MICROS PERIPHERALS AND INTERFACES.

JAN 2021 EXAM.

1 a) • ALU - ARITHMETIC LOGIC UNIT.

PERFORMS MATHEMATICAL + LOGIC OPERATIONS
+ CALCULATIONS. (1)

• PROGRAM COUNTER.

- POINTS TO NEXT PROGRAM STEP (1)

• TRISA (TRISB). - REGISTERS IN BANK 1
WHICH DEFINE THE PORTS AS INPUTS OR
OUTPUTS ON A BIT BY BIT BASIS (1).

b) MOST INSTRUCTIONS ARE EXECUTED WITHIN
1 INSTRUCTION CYCLE (4 CLOCK PERIODS) (1)

HOWEVER SOME INSTRUCTIONS CAUSE THE
PROGRAM COUNTER TO BE MODIFIED, OR
GIVE A POSITIVE RESULT TO A CONDITIONAL
COMMAND. IN THAT CASE 2 INSTRUCTION
CYCLES ARE REQUIRED. IE 8 CLOCK PERIODS (2)

c). RISC PROCESSORS HAVE A REDUCED
INSTRUCTION SET. (35 FOR PIC). THIS MEANS (1)
MOST INSTRUCTIONS ARE DESIGNED TO OPERATE
IN A SINGLE INSTRUCTION CYCLE. THE ADVANTAGE
OVER A CISC (COMPLEX INSTRUCTION SET COMPUTER)
EG PENTIUM. IS THAT IT CAN OPERATE QUICKLY. (1)
A DISADVANTAGE IS THAT COMPLEX OPERATIONS
REQUIRE MORE CODING EFFORT. (1).

d). TIME CRITICAL EVENTS CAN BE BEST PROGRAMMED
USING ASM. LANG. C, C++ RTL OFTEN RESULTS (1)
IN VERBOSE - INEFFICIENT CODE. DEPENDING
ON THE COMPILER. (1).

- 2). a) THE STACK IS AN AREA OF MEMORY USED TO STORE THE PROGRAM COUNTER WHEN INTERRUPTS OCCUR OR SUBROUTINES ARE CALLED. (1)

EG.

PC
000 CALL DELAY.
001 MOVW 0x00.F
002
→ DELAY 200 NOP
201 RETURN.

101 IS LOADED TO STACK.
200 IS LOADED TO PC

101 IS RETRIEVED FROM STACK AND LOADED TO PC. (1)

- b). SUBROUTINES ARE DISCRETE BLOCKS OF CODE THAT PERFORM A SPECIFIC FUNCTION WITHIN A PROGRAM. (1)

THEY CAN BE CALLED FROM OTHER SECTIONS OF CODE.

THEY ARE USED TO MAKE THE PROGRAM MORE EFFICIENT. OR COMPACT. (1)

THEY ALLOW FOR EASIER MAINTENANCE. (1)

THEY ALLOW FOR BETTER STRUCTURE. (1)

- c). EXTERNAL INTERRUPTS ARE CONNECTED TO B0 OR B4 TO B7. THEY ARE ENABLED BY SETTING BITS IN INTCON AND OPTION REGISTERS.. (1)

THEY CAN EITHER OPERATE ON A LEVEL (B0) OR A CHANGE OF STATE (B4 → B7)

THEY OCCUR ASYNCHRONOUSLY TO THE MAIN PROGRAM. ON ACTIVATION THEY CAUSE THE PROGRAM TO GO TO LOCATION 0004. (1)

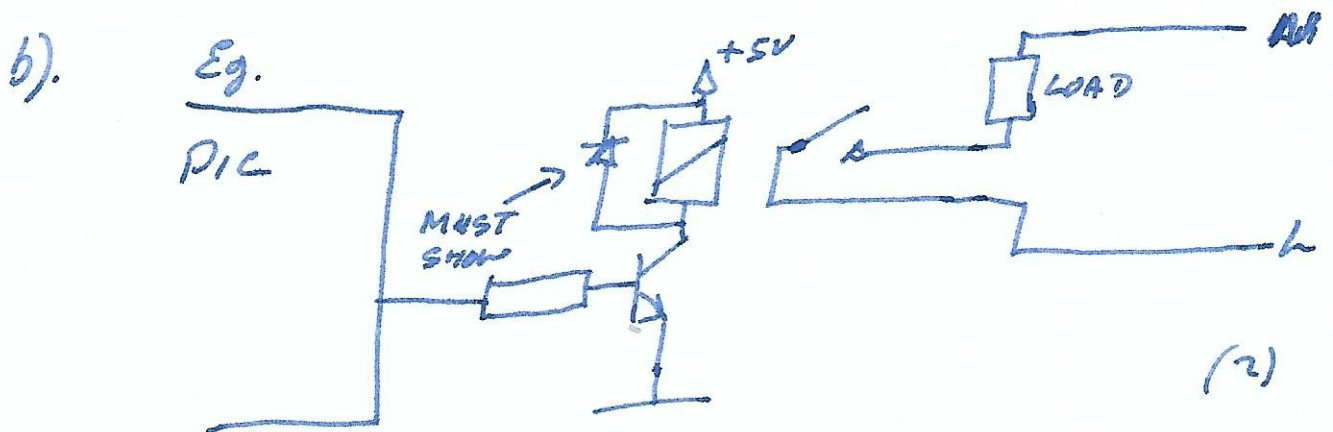
IN ORDER TO MAINTAIN PROGRAM OPERATION ON COMPLETION THE PROGRAM CONTEXT (W REG STATUS) NEED TO BE SAVED AND RESTORED. (1)

IT IS NECESSARY TO CLEAR THE INTERRUPT FLAG TO AVOID REPETITIVE INTERRUPT VECTOR. (1)

3 a). THE MAIN LIMITATIONS FOR CONNECTING LOADS TO THE OUTPUTS OF A PIC16F84A ARE:-

ONLY D.C. 0V & +5V.
LOW CURRENT. $\approx 20\text{mA}$ PER PIN. SOURCE
& 25mA PER PIN SINK. (1)

THERE ARE ALSO LIMITATIONS ON TOTAL POWER.

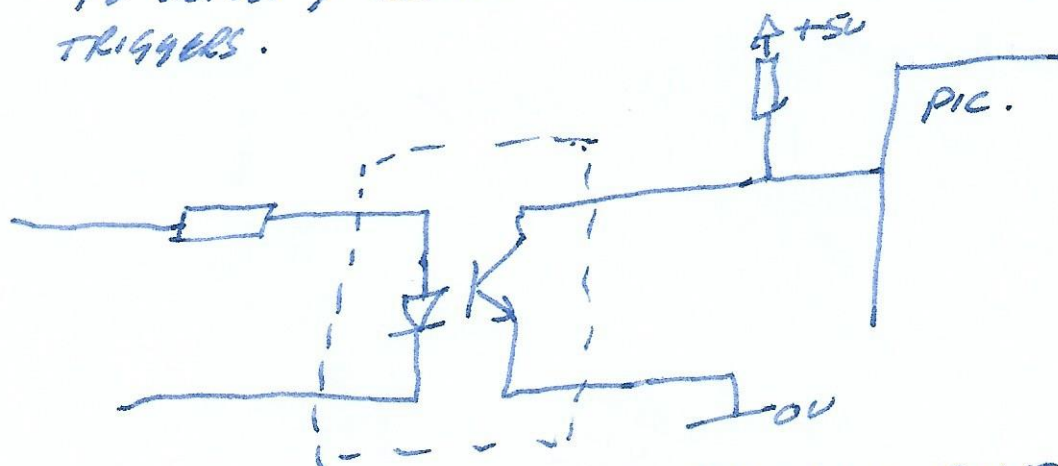


OTHER SOLUTIONS POSSIBLE.

c) SWITCHES OFTEN BOUNCE. GIVING FALSE SIGNALS.



A DEBOUNCE ROUTINE CAN BE USED TO DETECT / REMOVE THESE MULTIPLE TRIGGERS. (1)



OPTO ISOLATOR USED FOR ELECTRICAL ISOLATION (1)

d). 12 BIT A/D. HAS $2^n - 1$ STEPS.
 $= 4095$ STEPS

(1).

FOR 10V RANGE EACH STEP = $\frac{10}{4095}$

$= 0.002442$ V/STEP

(1).

$$\frac{6.5V}{0.002442} = 2661.75.$$

$$= 2662.$$

(1).

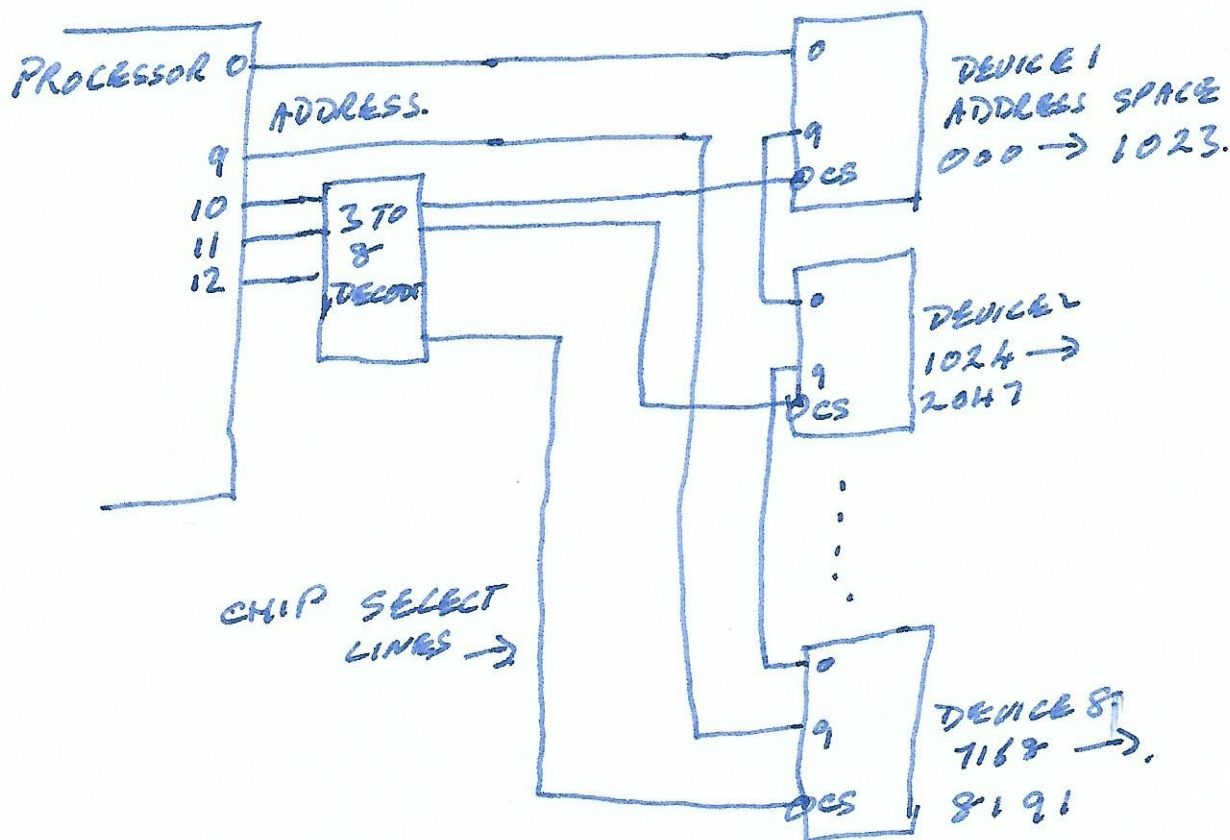
IN BINARY. 101001100110

(1).

4). a) 13 BITS = MEMORY OF 8192 BYTE.

EACH DEVICE IS 1024 $\therefore$ NEED 8 MEMORY DEVICES.

EACH 1024 BYTE REQUIRES 10 ADDRESS LINES.



DECODE.

A ₁₂	A ₁₁	A ₁₀	CS ₇	CS ₆	CS ₅	CS ₄	CS ₃	CS ₂	CS ₁	CS ₀
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

b). MEMORY ADDRESS 4699.

IN BINARY. 100 100 101 101 1

(1).

A₁₂ A₁₁ A₁₀ = CS₄.
1 0 0

(1)

ADDRESS SPACE 4096. → 5119.

A₉ → A₀.
1 0 0 101 101 1 = LOCATION 603.

SO LOCATION 603 DECIMAL IN
EN MEMORY DEVICE NO 5. (CS₄)
= MEMORY LOCATION 4699.

(1)

c). VON - NEUMANN ARCHITECTURE USES THE SAME
MEMORY + BUS FOR PROGRAM MEMORY
AND DATA MEMORY. THIS CAN LEAD TO BOTTLENECKS
AND THE POSSIBILITY OF PROGRAMS BEING CORRUPTED. (1)

HARVARD ARCHITECTURE HAS SEPARATE PROGRAM
MEMORY BUS AND DATA MEMORY BUS. (1)

5).a) DIRECT MEMORY ACCESS IS A MEANS BY WHICH AN EXTERNAL DEVICE CAN SHARE AND UPDATE MEMORY WITH THE MAIN PROCESSOR. THEN EXTERNAL DEVICE ACCESSES THE MEMORY WITH THE AID OF A DMA CONTROL FUNCTION. (11)

THE THREE MODES ARE.

BURST MODE. — THE DEVICE REQUESTS ACCESS THE PROCESSOR GRANTS ACCESS DEVICE TAKES CONTROL OF ACCESS (11) DEVICE RELINQUISHES CONTROL.

CYCLE STEALING — THE DMA CONTROLLER IS GIVEN ACCESS ON A CYCLE BY CYCLE BASIS. DEPENDING ON PROCESSOR GRANTING (11) ACCESS. — SLOWER THAN BURST MODE.

TRANSPARENT — THE DMA CONTROL RECOGNISES WHEN THE PROCESSOR IS NOT ACCESSING THE BUS'S AND THEN PERFORMS MEMORY OPERATIONS WITHOUT THE PROCESSOR BEING AWARE. — TIME TO COMPLETE TRANSFER DEPENDS ON PROCESSOR ACTIVITY. (11)

b) SYNCHRONOUS INTERFACES USE A COMMON CLOCK SIGNAL WHILE ASYNCHRONOUS INTERFACES DO NOT HAVE A COMMON CLOCK. Eg RS232. (11)

SYNC. → I²C. SPI ETC.

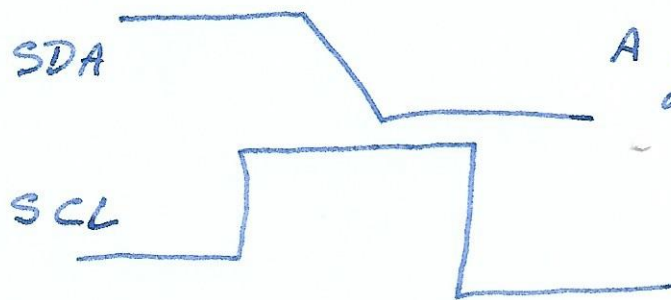
c). SPI IS POINT TO POINT. (11)
I²C IS POINT TO POINTS.

eg) SPI DOES NOT HAVE START + STOP BITS (11)
I²C DOES.

I²C INCLUDES ADDRESSING (11)
SPI USES CHIP SELECT.

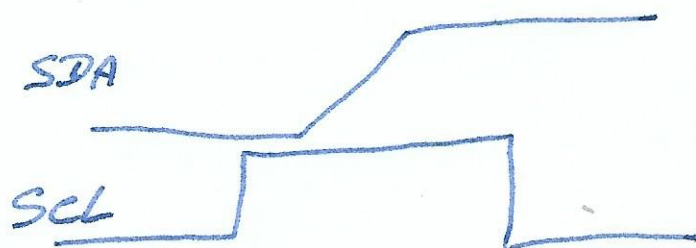
OTHER ANSWERS. POSSIBLE.

d) I²C START



A HIGH TO LOW TRANSITION
ON SDA WHILE SCL IS HIGH (1)

I²C STOP



A LOW TO HIGH TRANSITION
ON SDA WHILE SCL IS HIGH (1)